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ANNA UNIVERSITY (UNIVERSITY DEPARTMENTS)

B.E. Full Time - END SEMESTER EXAMINATIONS, May/June 2024

Electrical and Electronics Engineering
IV Semester
EE5401 - DIGITAL ELECTRONICS
(Regulation2019)

Time: 3 hrs Max.Marks: 100

CO1	To introduce the fundamentals of combinational and sequential digital circuit.
CO2	To study various number systems and to simplify the mathematical expressions using Boolean functions word problems.
CO3	To study implementation of combinational circuits using Gates` and MSI Devices.
CO4	To study the design of various synchronous and asynchronous circuits.
CO5	To introduce digital simulation techniques for development of application-oriented logic circuit.

BL – Bloom's Taxonomy Levels
(L1-Remembering, L2-Understanding, L3-Applying, L4-Analysing, L5-Evaluating, L6-Creating)

PART- A(10x2=20Marks)
(Answer all Questions)

Q.No	Questions	Marks	CO	BL
1	Convert 345.678_{16} to decimal	2	1	L3
2	Can a base for a number system be a fraction? Justify your answer	2	1	L3
3	Differentiate encoder and multiplexer.	2	2	L3
4	Draw the address enable signal for the memory address 82_H	2	2	L4
5	Define the term 'Moor's Model'.	2	3	L1
6	Recall the excitation table for JK flip flop.	2	3	L1
7	What are required conditions in designing Asynchronous sequential networks?	2	4	L2
8	If there is only one output column in the Transition Table for an Asynchronous sequential network, is it Moor's model or Mealey's Model?	2	4	L3
9	Give the number of Fanout of TTL logic circuits.	2	5	L1
10	Give the basic syntax for defining an architecture in VHDL.	2	5	L3

PART- B(5x 13=65Marks)

(Restrict to a maximum of 2 subdivisions)

Q.No	Questions	Marks	CO	BL
11.a	F = (A + B) (A + C). Using rules of algebra, reduce this equation step by step to simplest possible SOP form. Prove that LHS = RHS using tabulating method. Draw the circuits for both LHS and RHS.	13	1	L1
	OR			
11.b	Find the expression for the output variables using K-map	13	1	L3

Binary input			(Excess-3 code)-output			
B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	1	0

12.a	Explain the construction of three bit binary to gray code converter. Derive output variables (no need to draw the circuit)	13	2	L5
	OR			
12.b	Design a 4 to 2 priority encoder with output enable pin. Draw the circuit	13	2	L5
13.a	Give the block diagram, circuit diagram, truth table, and characteristic equation for i) T Flip Flop ii) SR Flip Flop	13	3	L2
	OR			
13.b	Analyze the given Synchronous sequential network by referring figure-1 and draw the state diagram	13	3	L2

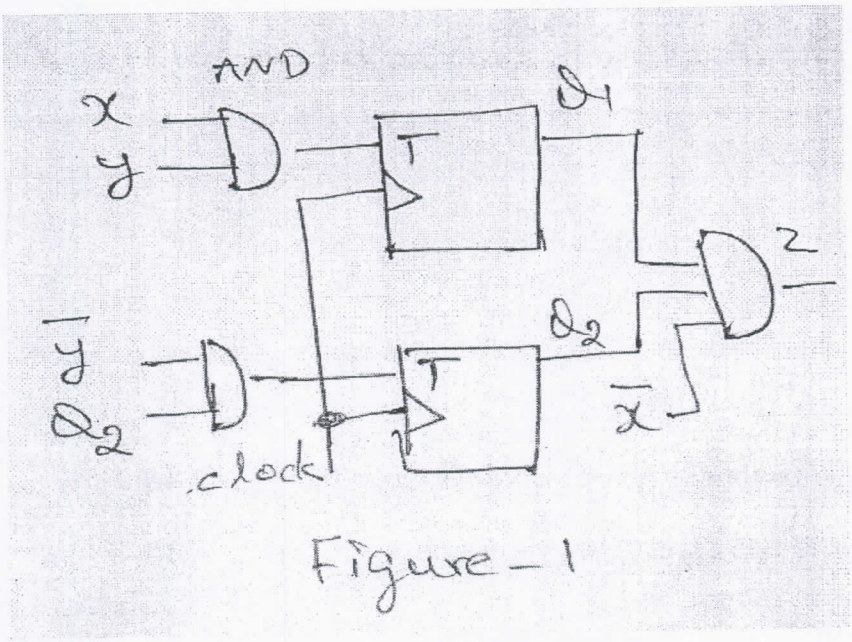

Figure – 1

14.a Analyze the given Asynchronous sequential network. by referring figure-2 and draw the flow diagram **13** 4 L4

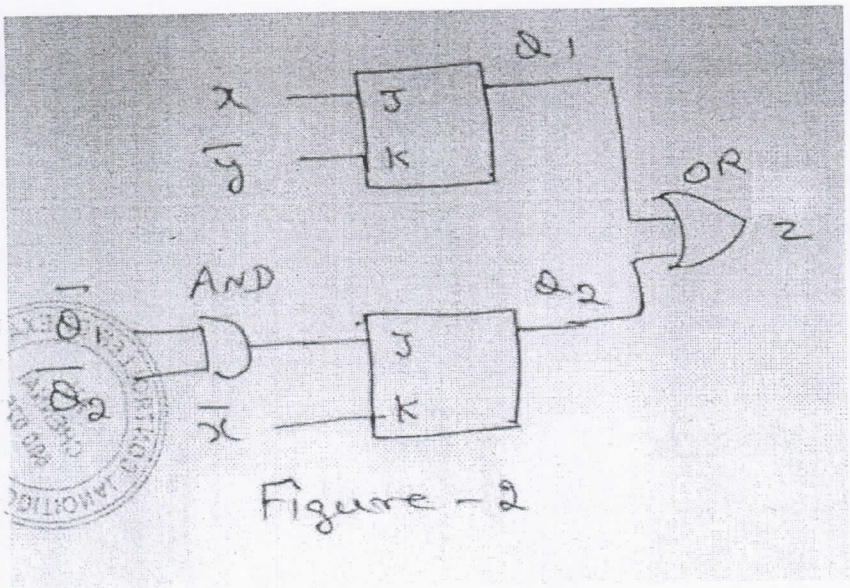

Figure – 2

OR

14.b Reduce the given state table. **13** 4 L4

P.S. Q_1 Q_2	N.S Q_1^+ Q_2^+		output	
	x=0	x=1	x=0	x=1
a	d	a	0	0
b	e	b	0	0
c	g	f	0	1
d	a	d	1	0
e	a	d	1	0
f	c	b	0	0
g	a	e	1	0

15.a	Draw and explain the operation of DTL and TTL logic circuits.	**13**	5	L3
	OR			
15.b	Draw and explain the operation of NMOS device.	**13**	5	L3

PART- C(1x 15=15Marks)

(Q.No.16 is compulsory)

Q.No	Questions	Marks	CO	BL
16	Draw the truth table for three digit - up counter and implement the circuit using D flip flop	**15**	5	L6